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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/938,163	09/26/97	TRAN H	TI-19819

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EXAMINER	
LE,D	
ART UNIT	**PAPER NUMBER**
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/938,163	Applicant(s) Tran
	Examiner Don Le	Group Art Unit 2819

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Claim Rejections - 35 USC § 112

1. Claims 3 and 10-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3, line 3 recites the limitation "the status of said precharge node" lacks antecedent bases. "The status" is not recited anywhere in claim 1.

Claims 10 and 11, line 3 recites the limitation "said second transistor". In accordance with the disclosure, applicant figure 4 shows one of the pair of transistors is coupled to the control electrode of the first transistor. It does not couple to the control electrode of the second transistor.

Claims 12 and 13 are indefinite base on their dependency of indefinite claims 10 and 11.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 1-9 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nowak et al. (US 5,831,452).

4. With respect to claim 1, figure 5B of Nowak shows a logic circuit comprising:

a precharge node (B) for retaining one of a high signal state and a relatively low signal;

an input node (INP);

a first transistor (T1) of one of n-channel or p-channel type having a control electrode and a current path coupled between a source of power and said precharge terminal;

a second transistor (T6) of the other of n-channel or p-channel type having a current path coupled between said input terminal and said control electrode of said first transistor and a control electrode; and

circuitry (T2, T5 and 10) coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node to control current flow in said current path of said second transistor.

5. With respect to claim 2, figure 5B of Nowak shows the logic circuit further including a pair of transistors (A1 and A2) having serially connected current paths, said serially connected current paths being coupled between said precharge node and a reference source.

6. With respect to claims 3-6, figure 5B of Nowak shows the circuitry coupled to said control electrode of said second transistor and responsive to the signal of said precharge node includes an inverter (10) having an input coupled to said precharge node (B) and an output (OUT) and a feedback circuit coupled between said output and said control electrode of said second transistor.

7. With respect to claim 7, figure 5B of Nowak shows the circuit further including a third transistor (T7) of said one of n-channel or p-channel type coupled between a source of power and

said control electrode of said second transistor and responsive to a said low signal at said output terminal to maintain said first transistor in an inactivated state.

8. With respect to claims 8 and 9, figure 5B of Nowak shows the circuit further including a fourth transistor (T2) of said one of n-channel or p-channel type coupled between a source of power and said precharge node and responsive to said low signal at said output terminal to maintain said precharge node at said high signal state.

9. With respect to claim 15, figure 5B of Nowak shows a domino logic circuit comprising:

an input terminal (INP);

a precharge node (B);

a first switch (T1) responsive to a second switch (T6) sensing one of a high or low voltage at said precharge node to charge said precharge node; and

said second switch responsive to said one of a high or low voltage at said precharge node to control said first switch charging said precharge node.

10. With respect to claim 16, figure 5B of Nowak shows the first switch (T1) in a p-channel transistor and the second switch (T6) is an n-channel transistor.

11. With respect to claims 17 and 18, figure 5B of Nowak shows the circuit further including an output terminal (OUT), an inverter (10) coupled between said precharge node (B) and said output terminal and feedback circuitry coupled between said output terminal and coupled to said second switch (T6) to provide said charge state of said precharge node to said second switch.

12. With respect to claims 19 and 20, figure 5 of Nowak shows the circuit further including a pair (T3 and T4) of transistors having serially connected current path, said serially connected current path coupled between said precharge node and a reference source.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak in view of Ling et al. (US 4,700,086).

15. With respect to claims 10 and 11, the apparatus of Nowak does not specifically show one of the pair of transistors is coupled to the control electrode of the first transistor. Figure 4 of Ling shows a logic circuit having one of a pair of transistors (X5 and 20) coupled to a control electrode of a first transistor (18) for the purpose of controlling on/off operation of the logic circuit. It would have been obvious to one of ordinary skill of art at the time the invention was made to have coupled one of the pair of transistors of Nowak to the control electrode of the first transistor as taught by Ling for the purpose of faster switching of on/off operation of the logic circuit.

Allowable Subject Matter

16. Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is an examiner's statement of reasons for allowance:

with respect to claims 12 and 13, in addition to other limitations in the claims, the prior art does not show a logic circuit having a fifth transistor coupled in parallel with a second transistor with a control electrode coupled to a precharge node.

With respect to claim 14, in addition to other limitations in the claim, the prior art does not show a logic circuit having one one of the claimed pair of transistors coupled to a portion of a current path to a second transistor remote from a first transistor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. Murakami et al. (US 5,015,890) disclose a logic circuit having first and second transistors and feedback circuitry.

B. Kikuda et al. (US 4,914,326) disclose a logic circuit having a feedback delay.

C. Sharpe-Geisler (US 5,457,404) disclose a logic circuit having first and second transistors and feedback circuitry.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don Le, whose telephone number is (703) 308-4890. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)308-0956.

Don Le

Art Unit 2819

May 19, 1999

Jon Santamauro
Primary Examiner